METHODS FOR MAKING COPPER AND OTHER METAL INTERCONNECTIONS IN INTEGRATED CIRCUITS

Field of Invention

The present invention concerns methods of semiconductor device or integrated circuit manufacturing, particularly methods of forming interconnects from copper and other metals.

Background of the Invention

Integrated circuits, the key components in thousands of electronic and computer products, are interconnected networks of electrical components fabricated on a common foundation, or substrate. Fabricators typically use various techniques, such as layering, doping, masking, and etching, to build thousands and even millions of microscopic resistors, transistors, and other electrical components on a silicon substrate, known as a wafer. The components are then "wired," or interconnected, together to define a specific electric circuit, such as a computer memory.

Interconnecting millions of microscopic components typically entails covering the components with an insulative layer, etching small holes in the insulative layer to expose portions of the components underneath, and digging trenches in the layer to define a wiring pattern. Then, through metallization, the holes and trenches are filled with metal to form line-like wires between the components. The wires are typically about one micron thick, or about 100 times thinner than a human hair.

Aluminum and its alloys with silicon and copper are the most common metals used for the wires, or interconnects. However, at sub-micron dimensions, that is, dimensions appreciable less than one micron, aluminum-based interconnections present not only higher electrical resistances which waste power and slows down the integrated circuit, but also poor electromigration resistance

which lets the aluminum diffuse, or leach, into neighboring structures. This diffusion degrades performance of an integrated circuit, ultimately undermining its reliability. Thus, there is a need to form sub-micron interconnections from metals other than aluminum.

Copper appears, because of its lower electrical resistivity and higher electromigration resistance, to be a promising substitute for aluminum. However, conventional interconnection techniques have proven impractical for making sub-micron interconnects from copper, specifically for filling the quarter-micron-wide holes and trenches thought necessary for tomorrow's smaller, more densely-packed integrated circuits.

For example, when using the conventional metallization technique of sputtering to fill trenches with copper, copper atoms spray out widely (in comparison to the width of the trenches), stick to the sidewalls of the trenches, and then to each other, eventually building bridges, or closures, across a trench and ultimately leaving voids, or wormholes, in the resulting copper wire. Similarly, when sputter-filling small holes with copper, the resulting vias are riddled with voids. These voids not only reduce the physical integrity of the copper interconnects, but also increase their electrical resistance significantly.

One attempt at solving this problem is the Hirao technique disclosed by S. Hirao and his coworkers in their article "A Novel Copper Reflow Process Using Dual Wetting Layers" (Symposium on VLSI Technology, Digest of Technical Papers, pp. 57-58 (1997)). The Hirao technique forms a trench and two diffusion barriers, one inside the trench and the other outside the trench. The inside diffusion barrier consists of a high-wetting, titanium-tungsten, and the outside diffusion barrier consists of a low-wetting, silicon-nitride. Next, the Hirao technique conventionally sputter deposits copper over both the inside and outside diffusion barriers, and afterward executes a reflow step, which heats the copper to 450°C for 5 minutes in a vacuum. During reflow, the copper flows off the low-wetting, outside

diffusion barrier into the trench, where the high-wetting diffusion barrier, to which copper easily sticks, promotes voidless copper consolidation.

Unfortunately, the Hirao technique suffers from at least four drawbacks. First, the technique is time-consuming and inefficient, particularly during formation of the outside diffusion barrier. Forming the outside diffusion barrier entails depositing a sheet of silicon nitride on an insulative layer and then masking and etching through the barrier into the insulative layer to form the trench. This etching is especially time consuming because it must dissolve not only the silicon nitride but also the insulative layer. Second, the Hirao technique forms the inside diffusion barrier using conventional sputtering which fails to yield a lining that conforms accurately to the profile of the trench or hole, ultimately yielding a deformed copper conductor with a smaller cross-section and therefore greater resistance. Third, conventional sputtering deposits the inside barrier material both inside and outside the trench, necessitating an additional scrubbing or polishing step to remove the material outside the trench. Not only is this additional scrubbing step time consuming, but it very likely wears away some of the silicon nitride material forming the outside barrier layer, reducing its effectiveness. Fourth, to control wettability of the barrier layers, the Hirao technique describes an argon-plasma treatment, another time-consuming step that further impairs its practicality.

Accordingly, there remains a need for practical methods of making low-resistance, high-reliability copper interconnections.

Summary of the Invention

To address these and other needs, the inventors have developed new methods of filling holes and trenches with copper or other desirable metals. Specifically, one embodiment of the invention entails forming a trench or hole, ionized-magnetron sputtering a first material inside the trench or hole, and then jet-vapor depositing a second material outside the trench or hole. Another step fills the trench or hole with copper or other suitable metal.

The preferred embodiment conducts the jet-vapor deposition at an acute incident angle, and uses ionized-magnetron sputtering to fill the trench or hole with copper. In addition, the preferred first material consists essentially of a high-wetting diffusion-barring material, such as tungsten (W), titanium-tungsten (TiW), or titanium nitride (TiN). The second material consists essentially of a low-wetting diffusion-barring material, such as a silicon nitride (SiN) or a zinc oxide (ZnO). Moreover, after filling the trench or hole with copper, the preferred method heats, or anneals, the copper-filled trench, thereby promoting voidless consolidation of the copper within the trench or hole.

The preferred embodiment provides at least two advantages over the Hirao and related techniques. First, in contrast to conventional magnetron sputtering, ionized-magnetron sputtering of the first material and the conductor metal forms a trench lining and a metal conductor that more accurately conforms to the trench profile, thus increasing cross-sectional area of the conductor and ultimately reducing its electrical resistance. Second, jet-vapor deposition at an acute incident angle prevents deposition of the second material into the trench or hole and therefore eliminates not only the time-consuming step of etching through the second material to form the trench or hole, but also the time-consuming step of scrubbing deposited material off areas outside the trench or hole.

Brief Description of the Drawings

Figure 1 is a cross-sectional view of an integrated-circuit assembly;

Figure 2A is a cross-sectional view of the Figure 1 integrated-circuit assembly after formation of an insulative layer and a trench;

Figure 2B is a top view of the Figure 2A integrated-circuit assembly, showing relative position of the trench;

Figure 2C is another cross-sectional view of the Figure 2A integrated-circuit assembly, taken along line C-C to show depth and width of the trench;

Figure 3 is a cross-sectional view of the Figure 2A assembly after formation of two diffusion barriers;

Figure 4 is a cross-sectional view of the Figure 3 integrated-circuit assembly after formation of a metal layer;

Figure 5 is a cross-sectional view of the Figure 4 assembly after removal of a portion of the metal layer;

Figure 6A is a cross-sectional view of the Figure 5 assembly taken along line A-A after formation of an insulative layer and a via hole;

Figure 6B is a top view of the Figure 6A assembly, showing relative position of the via hole;

Figure 7 is a cross-sectional view of the Figure 6A assembly after formation of two diffusion barriers and another metal layer; and

Figure 8 is a cross-sectional view of the Figure 7 assembly after removing a portion of the metal layer.

Description of the Preferred Embodiments

The following detailed description, which references and incorporates Figures 1-8, describes and illustrates one or more specific embodiments of the invention. These embodiments, offered not to limit but only to exemplify and teach the invention, are shown and described in sufficient detail to enable those skilled in

the art to practice the invention. Thus, where appropriate to avoid obscuring the invention, the description may omit certain information known to those of skill in the art.

Figures 1-8 show a number of preferred integrated-circuit assemblies, which taken collectively and sequentially, illustrate the preferred method of the present invention. The method, as shown in Figure 1, begins with a known integrated-circuit assembly or structure 10, which can be within any integrated circuit, a dynamic-random-access memory, for example. Assembly 10 includes a substrate 12. The term "substrate," as used herein, encompasses a semiconductor wafer as well as structures having one or more insulative, conductive, or semiconductive layers and materials. Thus, for example, the term embraces silicon-on-insulator, silicon-on-sapphire, and other advanced structures.

Substrate 12 supports a number of integrated elements 14, preferably transistors 14a and 14b. Transistors 14a and 14b are covered by an insulative layer 16, which preferably comprises silicon oxide, nitride, or oxynitride. Layer 16 includes two aluminum vias 16a and 16b electrically connected to respective transistors 14a and 14b. Although omitted from Figures 1-8 for clarity, assembly 10 preferably includes a titanium-nitride diffusion barrier between vias 16a and 16b and transistors 14a and 14b.

The first step, exemplified in Figure 2A, entails forming a one-micron-thick insulative layer 18 atop layer 16 and then forming a trench 20 which will ultimately define a desired conductor for connecting vias 16a and 16b. Layer 18, which preferably comprises silicon oxide, may be made using any deposition method. Trench 20 may be made using any selective-material-removal technique, although reactive-ion etching is preferred.

Figure 2B presents a top view of the assembly, showing the relative position of trench 20, and Figure 2C presents a cross-section along line C-C, showing depth 20d and width 20w of trench 20. In the preferred embodiment, trench 20 is less than 0.25 microns wide and at least one micron deep. Other defining features of trench

20 include two substantially parallel longitudinal edges, or perimeter lines, 20p and 20q, which are spaced according to width 20w, and terminal edges 20a and 20b, which determine length of trench 20. The preferred embodiment places terminal edges 20a and 20b over respective vias 16a and 16b.

The next step, shown in Figure 3, a cross-section similar to Figure 2C, entails lining, or coating, trench 20 with an inside diffusion-barrier 22. In the preferred embodiment, diffusion barrier 22 has a uniform thickness ranging between 50 to 100 nanometers, and comprises tungsten (W), titanium-tungsten (TiW), titanium nitride (TiN), or other high-wetting copper-diffusion-barring material. To conform the inside diffusion barrier to the bottom and sidewalls of trench 22, the preferred method forms diffusion barrier 22 through ionized-magnetron sputtering. Ionized-magnetron sputtering more accurately conforms to the profile of trench 20 than conventional sputtering techniques. This ultimately increases the cross section of the desired conductor, and thus reduces its actual electrical resistance.

The next step entails coating the shoulder or external regions of trench 20 with an outside (relative trench 20) diffusion barrier 24. In the preferred embodiment, outside diffusion barrier 24 comprises a silicon nitride (SiN) or a zinc oxide (ZnO) and is approximately 50 to 100 nanometers thick. Moreover, diffusion barrier 24 has edges adjacent longitudinal edges 20p and 20q and terminal edges 20a and 20b of trench 20. In the preferred embodiment, these edges are substantially even, or flush, with the trench edges to promote optimal reflow of metal into the trench during subsequent annealing steps. In contrast to previous techniques (such as the Hirao technique described in the background) that apply a material on a layer and afterward mask and etch through the material to form a trench (or hole) bordered by the material, the preferred embodiment uses jet-vapor deposition, a high-velocity gas flow technique, to form the outside diffusion barrier after forming the trench, thereby avoiding the time-consuming step of etching through the barrier material.

To achieve this time-savings, the method changes the deposition angle of incidence from the conventional perpendicular incident angle to a glancing incident angle of approximately 86-88 degrees relative the surface plane of layer 18. This is shown as angle 24a in Figure 3. In the preferred embodiment, the angular relationship is achieved by tilting the integrated-circuit assembly. While maintaining this relationship between the jet-vapor line of deposition and layer 18, the method rotates the integrated-circuit assembly within a horizontal plane using a rotatable substrate holder (not shown). (However, if desired, a jet-vapor output nozzle may itself be rotated about an axis of the stationary assembly.) This procedure forms diffusion barrier 24 outside and not inside trench 20.

For more information on jet-vapor deposition, refer to U.S. Patent Nos. 4,788,082 to Schmitt entitled "Method and Apparatus for the Deposition of Solid Films of a Material from a Jet Stream Entraining the Gaseous Phase of said Material" and 5,256,205 to Schmitt, III et al. entitled "Microwave Plasma Assisted Supersonic Gas Jet Deposition of Thin Film Materials," both of which are incorporated herein by reference. An additional reference, also incorporated herein, is A.R. Srivatsa et al., "Jet Vapor Deposition: An Alternative to Electro-deposition," Institute of Materials (1994). Further information may also be obtained from the Jet Process Corporation of New Haven, Connecticut.

Next, to form a metal conductor, the method fills trench 20, as shown in Figure 4, by depositing a metal layer 26 over the trench and surrounding areas, preferably using ionized-magnetron sputtering. For the one-micron deep trench of the preferred embodiment, a minimum 1.2-micron-thick copper layer is deposited. Preferred conditions for the ionized-magnetron sputtering operation are: target power range of 10-30 kilowatts for a 200-300 millimeter diameter wafer (or integrated-circuit assembly), RF coil power at 3-5 kilowatts, negative DC bias of 100-200 volts, sputtering argon gas pressurized at 1-35 millitorrs. Ionized-magnetron sputtering, which provides greater acceleration of the metal deposition material than conventional sputtering, forces the metal to more closely conform to

the interior profiles of holes and trenches. This, in turn, reduces the subsequent annealing time and temperature necessary to achieve an effective reflow and consolidation of the metal into a conductor.

Following the metal deposition is an annealing step. In the preferred embodiment, annealing proceeds for about 5 minutes at approximately 400°C or for about 30 minutes at approximately 320°C in a hydrogen atmosphere. For more details on annealing in hydrogen, refer to T. Miyake et al., "Atomic Hydrogen Enhanced Reflow of Copper," Applied Physics Letters, Vol. 70, 1997, which is incorporated herein by reference. The integrated-circuit assembly is then planarized by chemical-mechanical polishing (CMP) to remove metal remaining outside the trench. Figure 5 shows resulting metal conductor 26', which electrically connects vias 16a and 16b and therefore connects transistors 14a and 14b. Formation of conductor 26' completes the first level of metallization.

Figure 6A, a cross-section taken along line A-A in Figure 5, shows that the second level metallization starts with formation of a one-micron-thick dielectric layer 28 and an approximately quarter-micron-diameter (or larger) via hole 28a. (However, the invention is not limited to particular dimensions.) To enhance performance, dielectric layer 28 should have a dielectric constant as low as possible. The preferred embodiment uses a porous silicon dioxide. (For details on forming this material, see U.S. Patent 5,470,801 entitled "Low Dielectric Constant Insulation Layer for Integrated Circuit Structure and Method of Making Same" which is incorporated herein by reference.) Hole 28a is preferably formed using reactive-ion etching. Figure 6B shows the position of hole 28a relative transistors 14a and 14b, vias 16a and 16b, and conductor 26' from the first metallization level.

The next steps form an inside diffusion barrier 30 and an outside diffusion barrier 32, both according to the preferred procedures noted above for barriers 22 and 24. Accordingly, formation of inside diffusion barrier 30 entails ionized-magnetron sputtering, and formation of outside diffusion barrier entails jet-vapor deposition at an acute incident angle. Afterward, the preferred method forms a

copper layer 34 over the inside and outside diffusion barriers using ionized-magnetron sputtering and then executes an annealing step. Figure 8 shows that the resulting integrated-circuit assembly includes a copper via 34' electrically connected to underlying conductor 26' and thus also connected to transistors 14a and 14b. Subsequent metallizations would follow similarly.

With completion of the desired number of metallization levels, the preferred method ultimately concludes by heat-treating the integrated circuit for one to six hours at a temperature between 100 and 200°C. This heat treatment, which preferably occurs after packaging the integrated circuit in a protective housing, ensures that the metallic structures have minimum resistivity.

Conclusion

The present invention overcomes at least two significant shortcomings of previous interconnection techniques, particularly the Hirao method (described in the background.) First, instead of conventional sputtering to form an inside diffusion barriers, one embodiment of the invention uses ionized-magnetron sputtering to obtain superior sidewall coverage of small via holes and trenches and ultimately yields structures with larger cross sections and thus lower electrical resistance. Second, instead of using conventional techniques which require forming a barrier layer and then etching through it to form a trench, another embodiment uses a tilted jet-vapor deposition which prevents formation of the barrier within the trench and thus eliminates the need to etch through the barrier to form the trench. Moreover, one embodiment of the invention uses zinc oxide, instead of silicon nitride, as an outside diffusion barrier.

The embodiments described above are intended only to illustrate and teach one or more ways of practicing or implementing the present invention, not to restrict its breadth or scope. The actual scope of the invention, which encompasses all ways of practicing or implementing the invention, is defined only by the following claims and their equivalents.